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Laser Micro-machining and Applications of Glasses in Optoelectronics (*Invited*)
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Compact BJT/JFET PTAT
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Laser Micro-machining and Applications of Glasses in Optoelectronics

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Abstract

For glass machining and laser-induced crystallization, neodymium:yttrium aluminum garnet(Nd:YAG) laser was used. In glass machining process, laser drilled hole can be created by laser ablation with transparent wavelength of 1064nm. To create laser-induced silver metallic particles as seeds for nucleation in photosensitive glass containing Ag^{+} and Ce^{3+} ions, the pulse width and frequency of the used laser were 8 ns and 10 Hz, respectively. Heat treatment was conducted at 570ºC for 1 h, following laser irradiation, to produce crystalline growth, after which a $LiAlSi_3O_8$ crystal phase appeared in the laser-irradiated $Li_2O–Al_2O_3–SiO_2$ glass. For the present study, we compared the effect of laser-induced crystallization on glass crystallization with that of spontaneous crystallization by heat treatment.

Discussion 1 Introduction

Laser technology has been focused in many research fields for its powerful availability. Especially in glass, laser is very useful for the application of glass machining in spite of fragile property of it, thus the technology of laser treatment contribute to drilling, patterning, crystallization, 3-dimensional structuring, directional refractive index changes, waveguide writing and etc in glass. In this study, laser application fields to glasses are introduced, and our works, laser-induced crystallization and micromachining, are also demonstrated.

For laser machining in glass, it has been commonly known that Ultra-Violet (UV) laser is only effective because of its absorption in UV range. The existence of free electron which absorb photon energy by impurity insertion into a glass makes laser machining possible since reaction of avalanche ionization [1] despite of transparency of glass.

Ag and Au cations in the glass are the typical metallic ions to have the photosensitivity by UV beam irradiation with the help of Ce^{3+} ion as a sensitizer. The photosensitive mechanism in glasses is due to Stookey [2], and among others in the 1940s and 1950s. The electrons produced by the photo-ionization can reduce the ions to neutral metallic particles that play a role of nuclei in the glasses. Then, the subsequent heat-treatment can develop the microcrystalline consisting of the components in the glasses. In this study, Nd:YAG laser was used to induce photo-ionization in the glass, which contains Ag and Ce.

Discussion 2 Experimental Procedure

Lithium Aluminum Silcate Glass was prepared in this experiment. The batch was melted at 1550℃ for 2hrs, and held at 1500℃ for 2hrs for refining. The melts were cooled rapidly by being poured onto a carbon plate to prevent reduction and precipitation of silver.

The glass was sliced in 2mm thick and polished finely to be irradiated with Nd:YAG laser[3],[4]. The glass specimen were irradiated with 355nm and 1064nm wavelength. The parameters of the 355nm laser were 9ns pulse width, 10Hz frequency and 90mJ/cm^2/pulse, and 1064nm laser was 200ns pulse width, 50Hz frequency and 1.1J/cm^2/pulse .

After 355nm laser irradiation, heat treatment at 570℃ for 1hr was carried out to precipitate crystal phases in the glasses. We have observed drilled hole and growth of crystal phases in the glass with Optical Microscope and Scanning Electron Microscope. X-ray diffraction analysis (SIMATZU, DX-D1) was adopted to define crystals precipitated in the laser-irradiated area in the glasses.

Discussion 3 Results and Discussion

Fig.1 shows glass surface after 1064nm wavelength laser ablation with the noted energy. In the fig. 1, each hole was created by one pulse ablated through focusing lens and could achive uniformaty in drilling glass matrix. The photograph was taken by optical microscope.

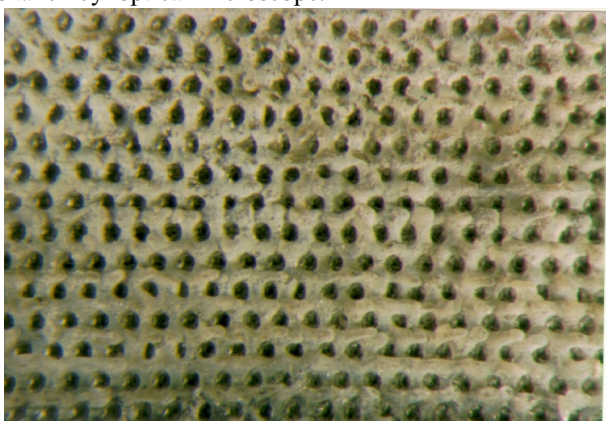

Fig. 1 Laser ablated glass surface with 200ns pulse width, 50Hz frequency and energy of 1.1J/cm2/pulse

Figure. 2 shows DSC(differential scanning calorimeter) traces of the non-laser irradiated glass and laser irradiated glass. Though the exothermic peaks are located in the area of 620, we adopted 570℃ for the crystallization as starting temperature of the exothermic peaks due to more sophisticated comparison of the crystallizations caused by laser induced and spontaneous nucleation. In fig. 2, we found that the glasses are showing the different intensities of the exothermal peaks of the crystallization in the glasses. The peak of the laser irradiated glass(a) locates around same temperature with non laser-irradiated glass, but has more exothermic energy comparing with the other. This phenomenon is due to that, we propose, the nucleation of laser treated glass has more nuclei with help of photochemical ionization, $Ce^{3+} + Ag^{+} \rightarrow Ce^{4+} +$

Ag^0, by photons of laser, which creates Ag metallic particles acting as seeds in the glass. Thus, it is considered that laser-induced nucleation by photons and spontaneous nucleation by heat treatment occur in the laser-irradiated glass at the same time, but only the spontaneous nucleation is happened in non laser-irradiated glass. As the result of it, laser irradiated glass have more exothermic energy of crystallization as we present in fig. 2.

Fig. 3 shows X-ray diffraction patterns of photosensitive glass containing Ag^+ and Ce^{3+}. In the laser irradiated glass (b) after heat treated, the $LiAlSiO_4$ crystals of lithium aluminum silicate was indicated in the angular range while the crystallization scarcely occurs in the non laser irradiated glass after heat treated. This result also agrees with it of the DSC patterns.

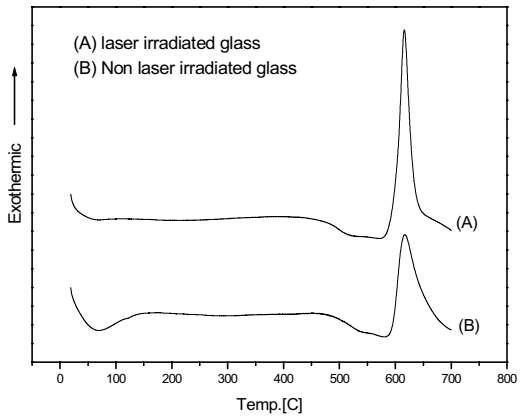

Fig. 2 DSC traces of laser irradiated glass(A) and non-laser irradiated glass(B). The exothermic peaks are indicating crystallization in each glass.

Fig. 4 is the photograph of Optical Transmission Polarized Microscope. In the fig. 4, the precipitated crystal phases are dispersed in the glass, which is observed by 200X magnitude. The white and black spots are indicating $LiAlSiO_4$ crystal phases created by laser induced nucleation and the smaller spots among them are also $LiAlSiO_4$ crystal phases resulted from spontaneous nucleation by heat treatment. After laser and heat treatment, any visible changes, such as crack, doesn't exist except color change toamber due to agglomeration of Ag.

Generally, two-step heat treatment for nucleation and crystallization is the typical process in most glass ceramics, but the proposed method for crystallization in this article is to utilize laser induced nucleation followed by one-step heat treatment. Thus, the author propose that the photo-ionization of Ce^{3+} by laser photons energy with 10-100mJ/cm^2 at 300-350nm wavelength, which is corresponding to ionization energy of Ce^{3+} by UV light for creation of novel metallic particles in a photosensitive glass, offers nucleation process in the glass while the spontaneous nucleation by heat treatment in non laser irradiated glass hardly effect on the crystallization due to not enough heating rate. Since any features or damages on the glass surface were not observed before heat treatment, we consider that the crystalline was created from silver metallic particles caused by the laser irradiation. We also proved that nanosecond pulse width laser beam with 355nm wavelength can create photo-ionization causing nucleation process. For the first time, we, in the author's knowledge, demonstrated that $LiAlSiO_4$ crystals can be precipitated by laser induced nucleation like as UV-light causing lithium methasilicate[13] or sodium fluoride crystals in typical photosensitive glass.

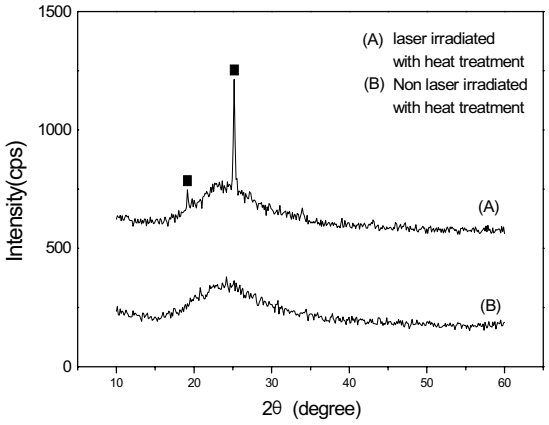

Fig. 3. X-ray diffraction patterns of photosensitive glasses containing Ag^+ and Ce^{3+}. Only sample(B) was laser irradiated with nanosecond pulses at a wavelength of 355nm with an energy of 90mJ/cm^2/pulse, and Each sample was heat-treated. $LiAlSiO_4$ is indicated in the figure.

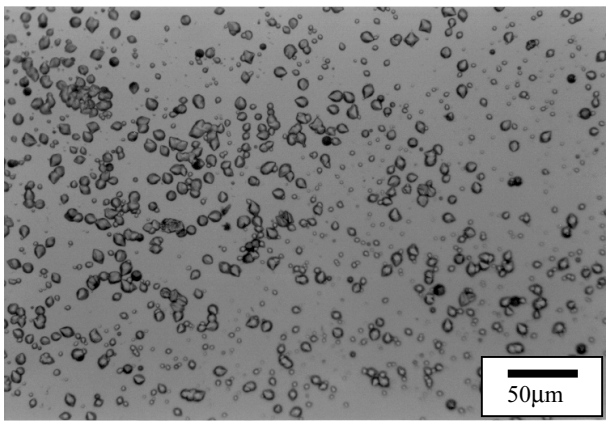

Fig. 4 Photograph of Optical Transmission Polarized Microscope for the photosensitive glass containing Ag^+ and Ce^{3+} heat-treated after the irradiation of 9 nano-second pulses at a wavelength of 355nm with 90mJ/cm^2 at 10Hz repetition for 20min.

Conclusions

We demonstrated laser drilling to glass matrix with transparable laser beam. It has prove that glass structuring is possible in practical application.

Also, in this study, 355nm laser irradiation induced the precipitation of $LiAlSiO_4$ crystals phases in the lithium aluminum silicate glass with laser induced nucleation process followed by heat treatment. This process for the crystallization is proposed to create Ag metallic seeds by photo reduction with electrons from Ce^{3+}, which is caused by laser photon energy. This method can be a unique and sophisticated way to control a desired crystal phase growth, and would give optically or electronically different properties distinguished from typical two-step heat treatment.

Acknowledgments

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Compact BJT/JFET PTAT

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Abstract

Research on a new compact BJT/JFET PTAT temperature sensor structure is reported. Equations describing sensor response are derived. The effects of important structure parameters are included. Measurements on fabricated test PTAT structures revealed reasonably good temperature response in a wide temperature range (-130°C to +100°C). At low temperatures (measured down to –200°C), considerable deviation from ideal PTAT response was detected. It is shown that deviation is due to the reduction of constant diode ideality factor n region, related to the free carriers freeze-out effect. JFET current generators, in spite of appreciable temperature dependence, do not include excessive nonlinearity.

1. Introduction

PTAT (Proportional To Absolute Temperature) silicon sensors[1] are an interesting class of temperature sensors due to peculiar properties of these structures such as proportionality to absolute temperature, accuracy, linearity, miniaturisation, measured range and others[2,3,4]. In this work we present an investigation of new PTAT sensor structures based on bipolar junction transistors (BJTs). Current generators are realized with junction field-effect transistors (JFETs), promising low noise properties[5].

Analysis of PTAT sensor response is reported. Derivation of basic equations describing PTAT sensors is given. Equations derived enable insight into proper sensor operation, resulting in better understanding and improved design of these structures.

Measurements of PTAT sensor temperature response, together with several structure parameters such as PN diodes forward characteristics and JFET current generators currents, on fabricated test PTAT structures revealed reasonably good response in the high temperature range (25°C to 100°C) and in the low temperature range (0°C to -130°C). Measurements at lower temperatures (down to –200°C) revealed considerable deviation from ideal PTAT response.

Analysis of measured results, based on derived equations, revealed that the reason for this deviation is the reduction of constant ideality factor n region, due to the free carriers freeze-out effect. It is also shown that in this case, JFET current generators in spite of appreciable temperature dependence, induce one order of magnitude smaller deviations.

2. BJT/JFET PTAT structure

Equivalent circuit of BJT/JFET PTAT sensor structure under observation is presented in Fig.1 (circuit inside dotted line). The heart of this PTAT structure are one small and one big BJT. Both transistors have a common base and collectors are realised with bulk/substrate region, differing therefore only in their emitter-base diodes. In majority of cases only emitter-base diodes are to be considered, with collector shorted to base. Therefore we replace, for transparency reasons, BJTs with their equivalent emitter-base diodes, as shown in Fig.1. Big transistor/diode D_2 is designed with emitter area ten times greater than the small diode D_1.

Current generators are realised with JFETs, described elsewhere[6]. Big JFET J_1 is designed with channel width-to-lenght ratio (W/L) ten times greater than the small JFET J_2.

Details of PTAT sensor application and measurement circuit is also shown in Fig.1. This circuit can be used for PTAT structure characterisation as well as for its application. Sensor supply voltage is provided by voltage source V_4. Sensor response, output voltage Δu_{BE} , is measured as the voltage difference between points V_2 and V_1. Base and collector/bulk regions of BJTs are in this case connected to the positive contact of supply voltage, therefore $u_{CB1,2} = 0$.

Current generators, providing two different currents i_1, i_2 for proper PTAT operation, are realised with JFETs J_1,J_2. As seen in Fig.1, both JFETs have Gate shorted to Source ($u_{GS1,2} = 0$), and therefore their currents are equal to their saturation current $I_{DSS1,2}$, provided supply voltage is adequate ie. at least one diode forward voltage drop higher than the according JFET saturation voltage.

Test BJT/JFET PTAT structures were designed and fabricated. Details of fabrication procedure are given elsewhere[6].

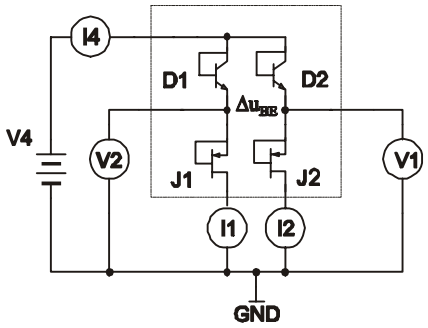


Fig.1. PTAT circuit

3. Analysis of PTAT operation

Current and voltage in an emitter diode, i_E and u_{BE} , can be related by[3]

$$i_E \cong \frac{1}{\alpha} I_{ES} \exp\left(\frac{q u_{BE}}{nkT}\right) \quad (1)$$

where we have included diode ideality factor n for improved description, α is transistor common base current gain, I_{ES} emitter diode saturation current, k Boltzmann constant and T absolute temperature.

The PTAT sensor response $\Delta u_{BE}(T)$, being the voltage difference between both emitter diodes (Fig.2), can therefore be written as

$$\Delta u_{BE}(T) = u_{BE1} - u_{BE2} = \left[n_1 \ln\left(\frac{i_{E1}}{\alpha_1 I_{ES1}}\right) - n_2 \ln\left(\frac{i_{E2}}{\alpha_2 I_{ES2}}\right)\right]\frac{k}{q}T \quad (2)$$

We introduce ideality factor difference $\Delta n_{21} = n_2 - n_1$ and substitutions

$$n_1 = n\,,\; n_2 = n + \Delta n_{21}\,,\; r_i = \frac{i_{E1}}{i_{E2}}\,,\; r_\alpha = \frac{\alpha_2}{\alpha_1}\,,\; r_S = \frac{I_{ES2}}{I_{ES1}} \quad (3)$$

So, response can be written as

$$\Delta u_{BE}(T) = \left[n\ \ln(r_i\ r_S\ r_\alpha) - \Delta n_{21} \ln\left(\frac{i_{E2}}{\alpha_2 I_{ES2}}\right)\right]\frac{k}{q}T \quad (4)$$

3.1. Ideal PTAT sensor

In this case, all sensor parameters are independent of temperature and are constant ie. have some fixed reference values

$$n = n_r\,,\; r_i = r_{ir}\,, r_\alpha = r_{r\alpha}\,, r_S = r_{Sr}\,, \Delta n_{21} = 0 \quad (5)$$

Response for ideal PTAT sensor from (4) is therefore

$$\Delta u_{BEid}(T) = \left[n_r\ \ln(r_{ir}\ r_{Sr}\ r_{\alpha r})\right]\frac{k}{q}T \quad (6)$$

and its sensitivity

$$S_{id} = \frac{d\,\Delta u_{BEid}}{dT} = \left[n_r\ \ln(r_{ir}\ r_{Sr}\ r_{\alpha r})\right]\frac{k}{q} \quad (7)$$

As expected, for ideal case PTAT sensor response is directly proportional to absolute temperature T and its sensitivity constant.

If we apply typical values for reference values of sensor parameters, determined by experiment as described later (n_r = 1.03, r_{ir} = 13.8, r_{Sr} = 13.5, $r_{\alpha r}$ = 1), we obtain from (7) typical valueof ideal PTAT sensitivity S_{id} = 0.46 mV/K .

3.2. Real PTAT sensor

In this case, sensor parameters are in general temperature dependent. Therefore, we write in general temperature dependence of a quantity in the form

$$x(T) = x_r + \Delta x(T) = x_r\left[1 + \frac{\Delta x(T)}{x_r}\right] \quad (8)$$

where x stands for any of the sensor parameters (n , r_i , r_S , r_α). In a good sensor, parameters variations are small ($\Delta x/x_r << 1$).

In order to avoid complex expressions, preventing transparency, we will study the contributions of nonideal parameters behaviour in real PTAT sensor for each parameter individually.

First, we assume $\Delta n_{21} = 0$, and return to this term later. We start our analysis with sensor sensitivity S, normalised for compactness of result by constant S_{id} from (7)

$$\frac{S}{S_{id}} = \frac{1}{S_{id}}\frac{d\Delta u_{BE}}{dT} = \frac{d(\Delta u_{BE}/S_{id})}{dT} = \frac{d}{dT}\left[\frac{n\ln(r_i\ r_S\ r_\alpha)}{n_r\ln(r_{ir}\ r_{Sr}\ r_{\alpha r})}T\right] \quad (9)$$

Taking into account temperature variations as given by second part of (8), and neglecting second and higher order terms (Δ^2, ..), we get

$$\frac{S}{S_{id}} = 1 + \Delta(T) + T\frac{d\Delta(T)}{dT} \quad (10)$$

where

$$\Delta(T) = \frac{\Delta n}{n_r} + \frac{1}{\ln(r_{ir}\ r_{Sr}\ r_{\alpha r})}\left(\frac{\Delta r_i}{r_{ir}} + \frac{\Delta r_S}{r_{Sr}} + \frac{\Delta r_\alpha}{r_{\alpha r r}}\right) \quad (11)$$

Second, we analyze the second term in (4), including the effect of ideality factor difference $\Delta n_{21} = n_2 - n_1$ on the PTAT sensor response. All other sensor parameters here are taken constant, at their reference values.

Fig.5 represents ideality factors n_1, n_2 dependence vs. voltage and temperature, calculated by differenciation following (1), from measured diodes characteristics graphically presented in Fig.4. Combining (4),(6) and (1) with assumptions described, response in this case is given by

$$\Delta u_{BE}(T) = \Delta u_{BEid}(T) - \Delta n_{21}\ln\left(\frac{i_{E2}}{\alpha_2 I_{ES2}}\right)\frac{k}{q}T = \quad (12)$$
$$= \Delta u_{BEid}(T) - \Delta n_{21}\left(\frac{u_{BE2}(T)}{n_2}\right)$$

Therefore, second term in (12) gives sensor deviation from ideal sensor response, due to Δn_{21} .

Equations (1) to (12) give the description of PTAT operation. One important conclusion can be drawn here - the basic condition for a good PTAT sensor is that all variations Δx in these equations, contributing to deviation from ideal PTAT should be minimised. Especially detrimental effects on PTAT response is diodes ideality factors mismatch Δn_{21} , because this contribution following (12) is entering directly in

linear form into equation for deviation. Other effects are masked through equations (11), (10) for sensitivity and their effects on response deviation are so attenuated. This point will be confirmed also experimentally by measured results on test PTAT structures.

In the following, the equations for PTAT response will be applied in two cases of practical importance: PTAT high temperature operation (25°C to 100°C) and PTAT low temperature operation (0°C to -200°C). Various effects contributing to deviation from linear, ideal PTAT response, will be studied.

4. PTAT high temperature operation

Measured response of PTAT sensor in high temperature range (25°C to 100°C) is given in Fig.2. Various effects described in Ch.3 that can contribute to the deviation of PTAT response will be analyzed in the following.

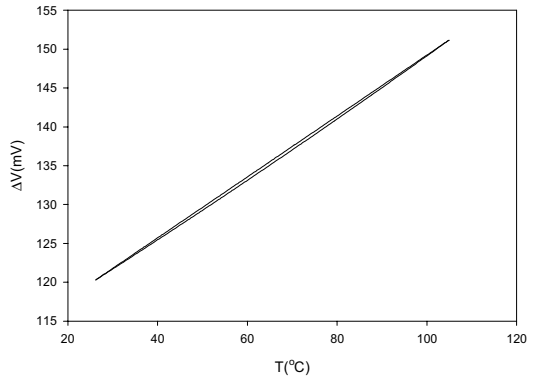


Fig.2. Measured PTAT sensor response in high temperature range

4.1. Effect of current ratio r_i

In this case we study only the effect of current ratio variation with temperature, $r_i(T) = i_1/i_2$, on the sensor response. All other sensor parameters are taken constant here, at their reference values (i.e. their variations $\Delta x = 0$).

Measured JFET currents and current ratio are represented in Fig.3. From measured current vs. temperature characteristics for JFETs, analytical relation for $r_i(T)$ can be obtained

$$r_i(T) = 13.77 - 3.77.10^{-3} K^{-1} (T - T_{\min}) = \\ = 13.77 [1 - 0.2731 0^{-3} K^{-1} (T - T_{\min})] \quad (13)$$

where T_{min} = 299.4K (= 26.2°C) is starting (minimal) temperature in these measurements. Comparing (8) and (13), we determine r_{ir} =13.77, $\Delta r_i(T)/ r_{ir}$ = -0.273 .10^{-3} K^{-1} (T – Tmin).

Taking all this into account, from (11) we obtain

$$\Delta(T) = \frac{1}{\ln(r_{ir}\, r_{Sr}\, r_{\alpha r})} \left(\frac{\Delta r_i}{r_{ir}} \right) = -5.23.10^{-5}\, K^{-1} \left(T - T_{\min} \right)$$

and

$$\frac{S}{S_{id}} = 1 + 0.015 + 1.04.10^{-4}\, K^{-1}\, T \quad (14)$$

Therefore, the influence of current ratio variation is twofold: sensitivity is larger for a constant value and also for a temperature dependent contribution leading to nonlinear response. Both contributions result in deviation of response from ideal PTAT case as we will see from the following. Inversion of (9) and integration gives

$$\int_{T_{\min}}^{T} d\Delta u_{BE} = \int_{T_{\min}}^{T} S\, dT = S_{id} \int_{T_{\min}}^{T} \frac{S}{S_{id}} dT \quad (15)$$

Applying (14) and integrating results in sensor response Δu_{BE} vs.temperature

$$\Delta u_{BE}(T) = \Delta u_{BE}(T_{\min}) + \\ + S_{id} \left[1.016 (T - T_{\min}) - 1.05.10^{-4} K^{-1} (T^2 - T_{\min}^2) \right] \quad (16)$$

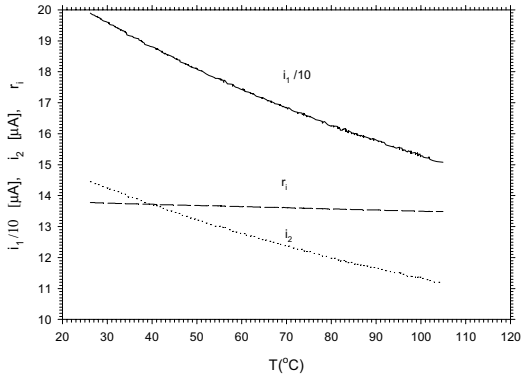


Fig.3. Measured JFET currents and current ratio

Therefore, due to current ratio variation with temperature $r_i(T)$, PTAT sensor response is shifted for a constant value. In addition, it contains one linear and one quadratic term of T, with magnitudes in our case of 0.73mV and 1.20mV. Therefore, measured values indicate that current ratio variation in this case is not critical.

4.2. Effect of saturation current ratio r_S

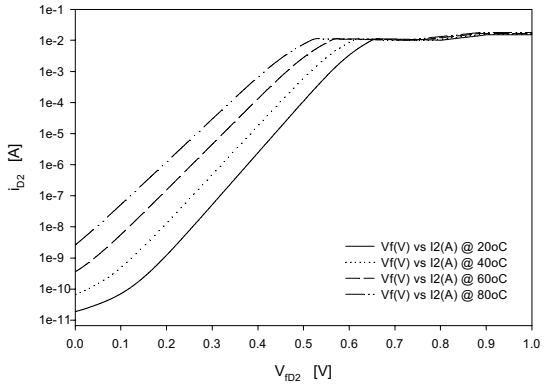
Saturation currents temperature dependence can be obtained from measured diodes temperature characteristics, Fig.4.

$$I_{S1}(T) = 2.67.10^{-32} \exp\left(0.142\, K^{-1}\, T\right) [A] \\ I_{S2}(T) = 3.60.10^{-31} \exp\left(0.142\, K^{-1}\, T\right) [A] \quad (17)$$

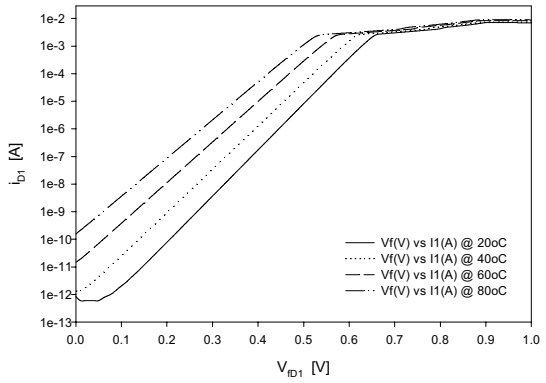
Therefore, saturation currents ratio r_s vs. temperature is given by

$$r_S(T) = \frac{I_{S2}(T)}{I_{S1}(T)} = 13.48 \quad (18)$$

and is temperature independent in our case. This confirms our expectations, due to the proximity of both emitter diodes on the same chip (matched diode pair). Consequently, $\Delta r_S = 0$, $\Delta(T) = 0$ and no effects on sensor response from this source.



a)



b)

Fig.4. Small diode (a) and big diode (b) current/voltage vs. temperature characteristics

4.3. Effect of current gain ratio r_α

For similar reasons as in the previous case, similar temperature dependence of common base current gains $\alpha_{1,2} \sim 1$ for both transistors is assumed. Therefore, $r_\alpha = \alpha_2/\alpha_1 \sim 1$ is constant and no effects on sensor response from this source are expected.

4.4. Effect of ideality factor n

As is shown in the next chapter, ideality factors n_1, n_2 are independent with temperature in our case. Therefore, $\Delta n(T) = 0$, $\Delta(T) = 0$ and no effects on sensor response from this source are expected.

4.5. Effect of ideality factor difference Δn_{21}

If we apply in (12) typical values estimated from our measurements, $\Delta n_{21} = n_2 - n_1 = -0.01$, $n_2 = 1.02 \sim 1$ (Fig.5), and $u_{BE2}(T)$ as determined from Fig.4, we get the response

$$\Delta u_{BE}(T) = \Delta u_{BEid}(T) - \Delta n_{21} u_{BE2}(T) = \Delta u_{BEid}(T) + \frac{u_{BE2}(T)}{100} \quad (19)$$

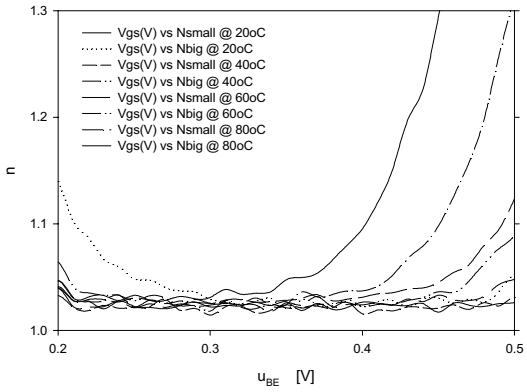


Fig.5. Ideality factors n_1, n_2

The effect of Δn_{21} term on sensor response is graphically presented in Fig.6. Interesting is the limiting case for low temperatures (T~0K). It is recognised that diode voltage limits to band gap voltage that is for silicon at 1.12V[7]. Therefore, due to Δn_{21}, we get a shift in response even at low temperatures that we indicate in Fig.6, due to 0K, as PTAT offset voltage Δu_{BEoff}. In this case, offset voltage Δu_{BEoff} is estimated from (19) to 11.2mV.

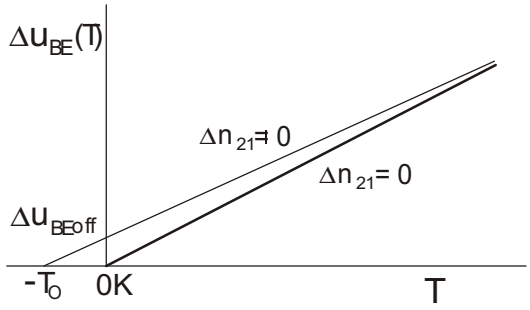


Fig.6. Response due to Δn_{21}

Alternativelly, this effect can be mathematically described as the shift of sensor characteristics to a new zero temperature $-T_0$ in Fig.6. The linear response is then described as $\Delta u_{BE}(T) = S_{lin}(T-T_0)$. From measurements, we determined S_{lin} =0.342mV/K and by extrapolation, zero temperature T_0 = 7K. Zero temperature can be evaluated (Fig.6) also as $T_0 = \Delta u_{BEoff}/S_{lin}$ = 33K. Difference between calculated and measured values indicates that there are others effects to be included. This will become more evident also in the next section.

5. Low temperature operation

Low temperature PTAT sensor response was measured in the temperature range 0°C to –200°C.

In the temperature range 0°C to –140°C, reasonably good sensor linearity is observed as shown in Fig.7.

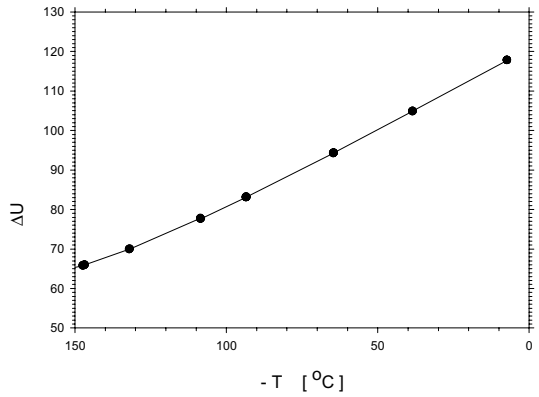


Fig.7. Measured PTAT sensor response (0°C to –140°C)

But, comparing measured PTAT sensor response to ideal PTAT sensor response in a wider temperature interval (0°C to –273°C), as shown in Fig.8, increasing deviation of measured response (dotted line) from ideal PTAT (straight line), when going down to low temperatures, is detected. In order to improve the understanding of sensor operation and therefore to enable optimised PTAT sensor structures design and fabrication, the effects responsible for this nonideal behaviour are analysed and discussed in the following.

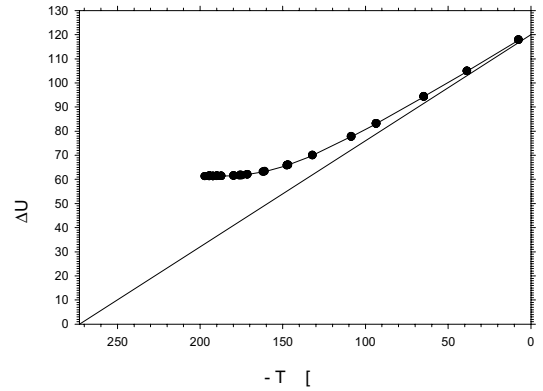
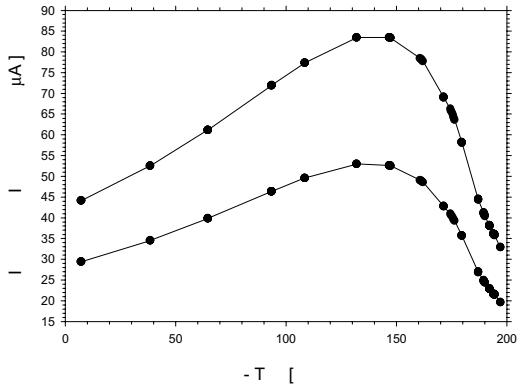


Fig.8. Measured and ideal PTAT sensor response (0°C to –273°C)

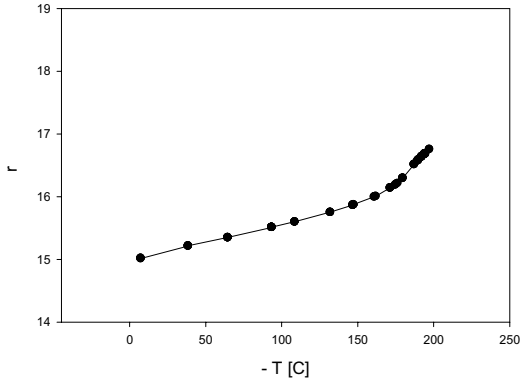
For similar reasons as described already in Ch.4, we concentrate here our attention on two main effects: temperature variation of JFET current generators (described by current ratio r_i) and nonideal PN diodes behaviour (described by ideality factors n).

5.1. JFET current generators temperature variation

Measured temperature dependence for currents of both JFET current generators are presented in Fig.9a. Current ratio r_i is presented in Fig.9b.



a)



b)

Fig.9. Measured JFET currents(a) and current ratio(b) vs. temperature

As seen in Fig.9a, going down to low temperatures, JFET currents are first increasing, due to mobility enhancement as a consequence of reduced charge carrier scattering[8]. Around -150°C currents begin to decrease, due to carrier freeze-out[8].

In spite of considerable temperature dependence of JFET generators(Fig.9a), according to our expectations, the current ratio is quite constant (variation only from 15 to 16 in the whole temperature range, Fig.9b), which is due to the matched JFET pair (i.e. made on the same chip).

The contribution to nonideality of PTAT response due to JFET current generators temperature dependence is determined following the derivation given in Ch.3. From measured results(Fig.9b), current ratio r_i variation with temperature is determined

$$\frac{\Delta r_i}{r_{ir}}(T) = \frac{K_{ri}}{r_{ir}}(-T) \qquad (20)$$

where $K_{ri} = 5{,}8.10^{-3}$ /°C and reference current ratio $r_{ir} = 15{,}0$ at some reference temperature T_r (= 0°C in this case).

Following (11), this induces function $\Delta(T)$

$$\Delta(T) = \frac{1}{\ln(r_{ir}\, r_{Sr}\, r_{\alpha r})}\left(\frac{\Delta r_i}{r_{ir}}\right) = 8{,}3.10^{-} \quad C^{-1}\left(-T\right) \qquad (21)$$

which, according to (10), generates sensitivity S deviation from ideal case

$$S = S_{id} + 2\frac{k}{q}\frac{K_{ri}}{r_{ir}}(-T) \qquad (22)$$

From known sensitivity, sensor response is derived again by integration ($\Delta u = \int S\,dT$)

$$\Delta u_{BE}(T) = \Delta u_{BE}(T_r) + S_{id}(T - T_r) - \frac{k}{q}\frac{K_{ri}}{r_{ir}}(T^2 - T_r^2) \qquad (23)$$

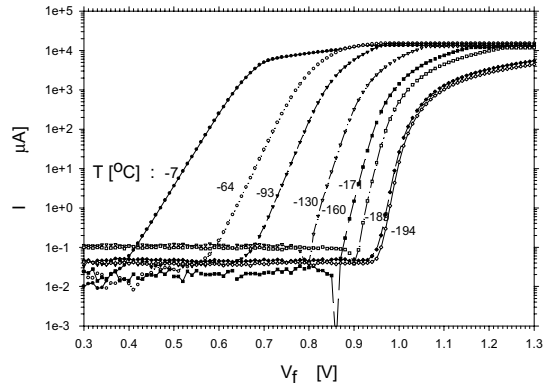
Therefore, response deviation from ideal PTAT sensor ε(T) is given by

$$\varepsilon T = \frac{k}{q}\frac{K_r}{r_r} T^2 - T_r^2 = 10^{-5}\, mV \frac{T^2}{C^2} \qquad (24)$$

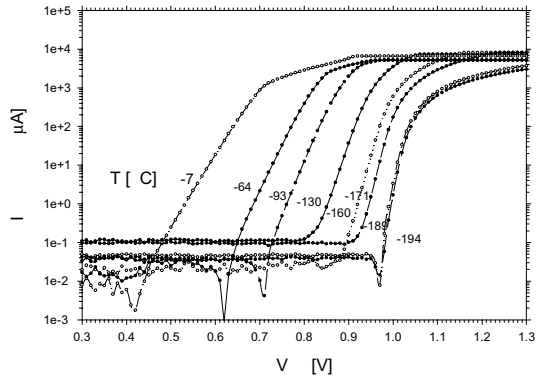
Calculations of response deviation due to current ratio r_i temperature variation, based on (24), revealed one order of magnitude smaller values than measured. Therefore, in spite of rather strong temperature dependence of JFET generator currents, there is no detrimental effects on PTAT properties. This is probably due to the fact that sensitivity and thus response of the PTAT sensor is related to current ratio variation indirectly through (10), (11).

5.2. Nonideal PN diodes behavior

Measured big and small diodes forward i/v characteristics for different temperatures are presented in Fig.10. Straight line in this semilog i/v plot indicates region of constant ideality factor n.



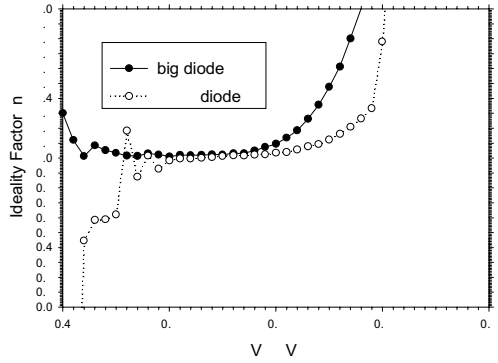
a) big diode



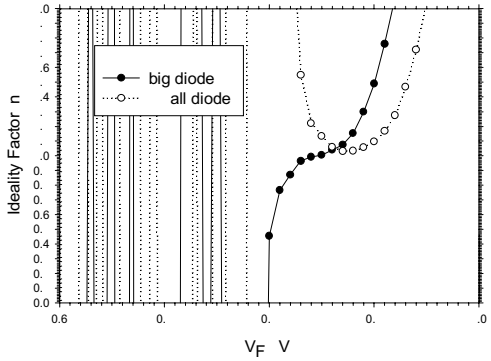
b) small diode

Fig.10. Measured diodes i/v characteristics vs. temperature

From (12) it follows that for good PTAT sensor response, the basic condition of equal ideality factors n for both diodes has to be fulfilled.



a) T = -7°C



b) T = - 130°C

Fig.11. Ideality factor n vs. diode operating point

Therefore, from measured tables for i/v diode characteristics we derived numerically ideality factors n at different temperatures. Some results are shown in Fig.11.

Around room temperatures, ideality factors are properly matched at diode actual operating point around 0.6V (Fig.11a), resulting in a good, linear PTAT response.

When going down to low temperatures, the constant ideality factor n range is decreasing and at lower temperatures (-130°C and lower) it is impossible to match even approximatelly n factors for both diodes (Fig.11b), which is the main condition for PTAT sensor linearity. Consequently, in this case it is not possible to realize linear PTAT temperature sensor, in agreement with our measurements.

The reason for the decay of constant ideality factor n region at low temperatures is again freeze-out of charge carriers, increasing thus the internal series resistance of diode. This results in nonideal PN diode forward i/v characteristics, leading finally to strong deviations of measured PTAT sensor response from ideal PTAT response.

Conclusions

Research on a new structure of PTAT temperature sensor based on BJT/JFET technology is reported. The effects of structure parameters of importance such as current ratio,

ideality factors and their difference, saturation currents ratio and current gain ratio are included. New equations for sensor response and sensitivity are derived. It is shown that JFET current generators, in spite of appreciable temperature dependence, operate well and do not contribute to excess nonlinearity. Measurements on fabricated test PTAT structures revealed reasonably good temperature response in a wide temperature range (-130^{o}C to +100^{o}C). At lower temperatures (measured down to –200^{o}C), considerable deviation from ideal PTAT response was detected. It is shown that deviation is due to the reduction of constant diode ideality factor n region, related to the free carriers freeze-out effect. The improved understanding of PTAT sensors will result in design and manufacture of new structures with improved properties

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A 3-D low-cost Packaging Technology for Ceramic Substrates

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Abstract

A 3-D packaging technology for ceramic substrates is described. Based on metallisation, mounting and soldering techniques, known from PCB mass production, it closes the gap between conventional thick-film hybrids and LTCCs with respect to packaging density and price. Samples manufactured on a lab scale show the potential of this technology. The reliability investigations comprehend peel off and thermal cycling tests.

The 3rd dimension in packaging

The continuously growing demand on packaging density in electronic devices cannot be realized by just decreasing line widths and clearances on one conducting layer but also requires an extension into the 3rd dimension. This lead to multilayer structures in the various fields of electronic packaging.

Printed Circuit Boards as multilayers are well established since the early 60s. Traditionally they are manufactured as individually processed single- or double-sided metallised FR 4 layers glued together by epoxy sheets (prepregs) in a high temperature, high pressure process. Then, after drilling, the outer layers are processed just like a double-sided PCB.

In recent years this technology was supplemented by sequentially built up multilayers, also referred as High Density Interconnection (HDI) PCBs.. Instead of a combination of exclusively rigid layers, the HDI boards are based on just one rigid PCB (which can be a conventionally manufactured multilayer) and a sequence of thin layers performed by application of liquid polymers and electroless and electroplating metallisation. The holes between the insulation layers can be achieved by various methods like laser drilling, plasma etching or liquid etching if a fotosensitive polymer is used. The HDI PCBs show a steep increase in production volume due to the increasing of complex, low weight and thin PCBs e.g. required in mobile phones.

On die level the enormous progress in packaging density has resulted in structures in the range of .1 µm, giving a strong impact on all other packaging levels to reduce their size significantly. Though state-of-the-art ICs already consist of 6-8 metallization layers, strong efforts are made to stack several dies which results in an even much higher packaging density. The interconnection between the individual dies is either done by soldering or by conductive gluing techniques. These vertically stacked dies can be housed e.g. in a standard BGA (Ball Grid Array) package as a CSP (Chip Size Package). Recently a folded stacked technology invented by Tessera and Intel is reported, which combines 3 dies in a CSP of just 1 mm height [1].

Looking at hybrids [2], low level multilayer structures are common since the early days of this technology. However, the number of layers on thick-film hybrids is somewhat limited to 3-4 due to problems in screen printing of the pastes on uneven surfaces. So the Low Temperature Cofired Ceramics (LTCC), originally introduced by Dupont as “Green Tape”, were developed. Based on soft “green” ceramic sheets, screen printed with conductor, resistor and sometimes dielectrica pastes for capacitors, after stacking and sintering (firing), LTCCs provide a densely packed hybrid with layer counts easily exceeding the number of 10. Examples for usefull applications of LTCCs are heart pace-makers.

Though established already in some niches, LTCCs are relatively expensive, preventing this technology to be used on a larger scale.

A technology which combines standard processes known from PCBs but applied to ceramic substrates could provide high interconnection densities at low costs. This technology, called RML (Reflow Soldered Multilayer), developed at the Georg-Simon-Ohm University of Applied Sciences in Nuernberg, Germany and investigated in some diploma theses, might solve the cost problem and additionally provides some other advantages.

The RML Technology

General considerations

The basic idea behind the RML technology was: it should be possible to build three-dimensional ceramic packages at much lower costs compared to LTCC. The good heat conductivity of ceramic material in general and its capacity to withstand high temperatures should allow the application of reflow soldering with a large process window. Moreover by restricting the whole technology to already established techniques, process costs and risks should be minimized.

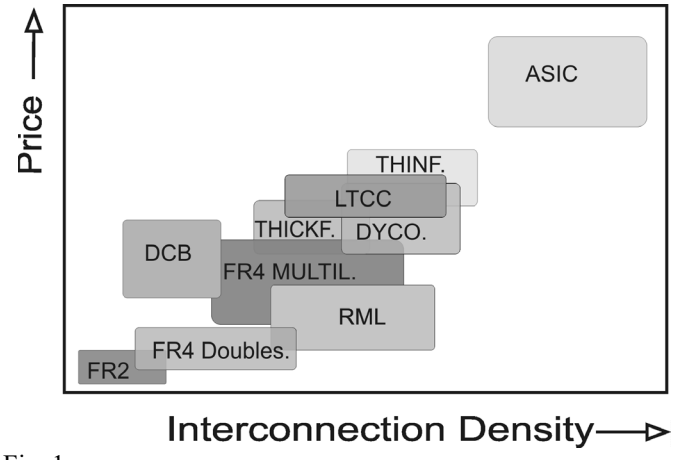

Fig. 1

So the RML technology is aimed at packaging densities near LTCC but at very competitive costs (fig. 1).

Packaging principle

The packaging principle of RML is shown in fig. 2. Individually processed ceramic substrates with metallized vias are screen printed with solder paste, stacked and reflow-soldered. After an additional solder past print on top of the stack, the components are mounted and reflow-soldered in a second soldering process.

The gap between the stacked layers is determined by the thickness of the solder paste, the weight of the substrates and, to a much smaller degree, by the soldering parameters. If an exactly defined clearance between adjacent layers is required, this can be achieved by spacers either remaining as part of the package or temporarily applied during the mounting and soldering process..

The insulation between the layers can be just air or any solid material which withstands the reflow temperatures.

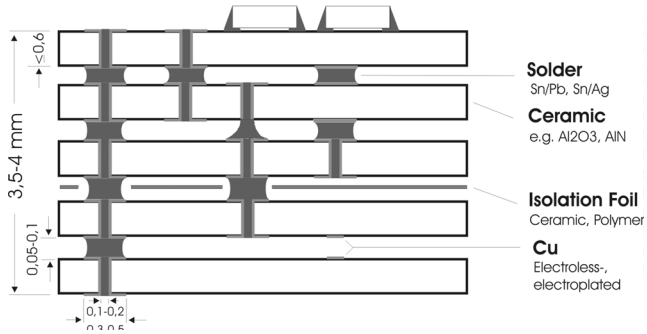

Fig. 2

As the individual substrates are processed *before* inter-connecting them, a wide variety of vias can easily be achieved: vias through the entire stack as well as any combination of blind and buried vias. This provides a very high flexibility in design.

The housing can be a standard package e.g. a QFP or the RML package is directly mounted to the PCB via a ball grid array on its bottom side.

Drilling

In our investigations we used 96 % alumina substrates as known from thick-film hybrids in standard thickness of .63 mm and .25 mm. Though the stacking of the individual substrates is done *after* sintering, the holes can be performed *before* or *after* the sintering process. Doing it before sintering is a very cost efficient method as all holes can be punched together in one step. We didn't investigate the punching, best suited for mass production, but did some investigations on drilling the holes mechanically. Placed on a wet rubber plate, the "green" substrates were drilled with a machine normally used for FR 4 PCBs at 60.000 rpm. Surprisingly, down to the available drill diameter of .1 mm, the results in .25 mm alumina were excellent. Though much slower than punching, mechanically drilling can be an alternative for small to medium scale production. Of course, drilling before sintering means that the shrinkage (approx. 15 %) during the sintering process has to be taken into account when creating the drill program.

After sintering, the holes have to be drilled with a laser. We used a Nd/YAG-laser and achieved in .63 mm substrates rather conically shaped holes with diameters of approx. .15 mm to .25 mm. A more cylindrical shape could be expected with a higher laser power.

Metallisation

Conductor or resistor structures on thick-film hybrids are achieved by sequentially screen printing and firing of metal or metal-oxide pastes. Though also conventional thick-film hybrids can be stacked in the RML technology, we followed a different approach. Instead we applied electroless and electroplating processes, normally used in PCB technology, to ceramic substrates with the goals of lower costs and smaller structures in mind.

As alumina is an electrical insulator, after cleaning the substrates were seeded with Sn/Pd followed by an electroless plating of copper in a thickness of approx. .5 µm and then enhanced by electroplating to 3-5 µm. The following steps could be the standard PCB technologies known as metal-resist subtractive or hot air leveling (HAL). technology

However we decided to modify the standard process sequence resulting in a combination of subtractive and semi-additive technologies. This novel metallization sequence, we call it "SELECTIN" (selectively electroplated tin), provides extremely flat electroplated solder pads connected by tracks passivated in a liquid process. The passivation acts as a solder resist and eliminates the problems accompanied by printing solder resist on fine-line structures. Moreover, SELECTIN ensures that the copper thickness in holes is always larger than on tracks, so the metallization in small holes with a high aspect ratio is no more a relibility risk.

Stacking and soldering

After the metallisation on the inner layers, solder paste is printed on top of each double-sided substrate, using stencils of e.g. 200 µm thickness. The stencil thickness defines the clearance between adjacent, interconnected layers. In our investigations, 200 µm solder paste resulted in a clearance of approx. 60 µm after reflow-soldering. Depending on the amount of solder, the load of the layers above and the soldering conditions, we got solder joints hour-glass or ton shaped

Besides eutectic tin/lead, also any leadless solder paste can be applied, even pastes with melting temperatures far beyond 250 ^{o}C, as in this stage the components are not yet mounted. The use of higher melting solder paste for the first reflow-solder process has the additional advantage that during the second reflow-soldering (e.g. with standard tin/lead) the inter-connection solder joints will not melt again.

After solder paste printing the substrates can be stacked either manually or automatically by a SMD pick&place machine. In both cases the area where the nozzle picks the substrate has to be kept free of solder paste. For small lateral dimensions of the substrates, the "solder paste keep out area" will be in the center. For larger substrates specifically designed nozzles will be required, picking up the substrates with four simultaneously operating nozzles near the substrate corners.

Stacking of the substrates is not critical with respect to accuracy if the solder joints are based on round pads. We observed a strong self-alignment effect during solder flow

which increased with increasing number of solder joints per area.

The reflow-soldering of the whole stack can be done in one process with any oven known from PCB production.

In the next step, the top layer of the stack has to be printed with solder paste where passive and active SMDs will be mounted on. The second reflow-soldering can be operated at a lower temperature as the first one if solder pastes with different melting points are used. It can be done with the same reflow-oven normally working with convection heat transfer, but also a method based on heat conduction method can be applied.

This method was used in the early days of thick-film hybrids when componenets were sensitive to overheating. The heat is transferred from infrared-heaters through a temperature-resistant belt (mostly Teflon) and through the substrate volume to the solder paste on top. Below the melting point, the solder paste has a high heat resistivity which avoids the heat flow through the paste into the componenet. So the component keeps cool until the solder paste is molten but then the process is already finished. This method is only applicable because of the good heat conduction of ceramics and the use of solder pastes with a higher melting point for the first soldering process.

Reliability

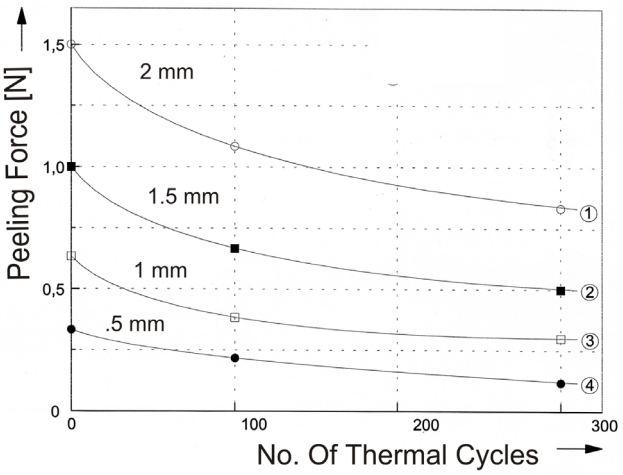

Fig. 3

Reliability tests were performed on 4-6 layer RML-packages approx. 20 mm x 20 mm in size to check the adhesion of the metallistion (5-15 µm Cu) and the integrity of the solder joints and vias. All test samples were exclusively soldered with standard eutectic tin/lead solder. For accelerated ageing the samples were cycled slowly from –20 °C to +100 °C up to 280 cycles.

As fig.3 shows, the peel off strength of tracks with different widths, decreases with increasing temperature cycles. However it is obvious that the drop is highest during the first 100 cycles and the peel off strength seems to stabilize at approx. 50 % of the initial value for longer cycling. We could not achieve peel off strengths of 1.1 N/mm specified for PCBs independent of acid or base pretreatments of the alumina surface. Though it has to be taken into account, that peel off specifications of large PCBs with heavy components cannot be 1:1 transferred to the much smaller ceramic RML modules, the electroless plating of ceramics is always a critical process.

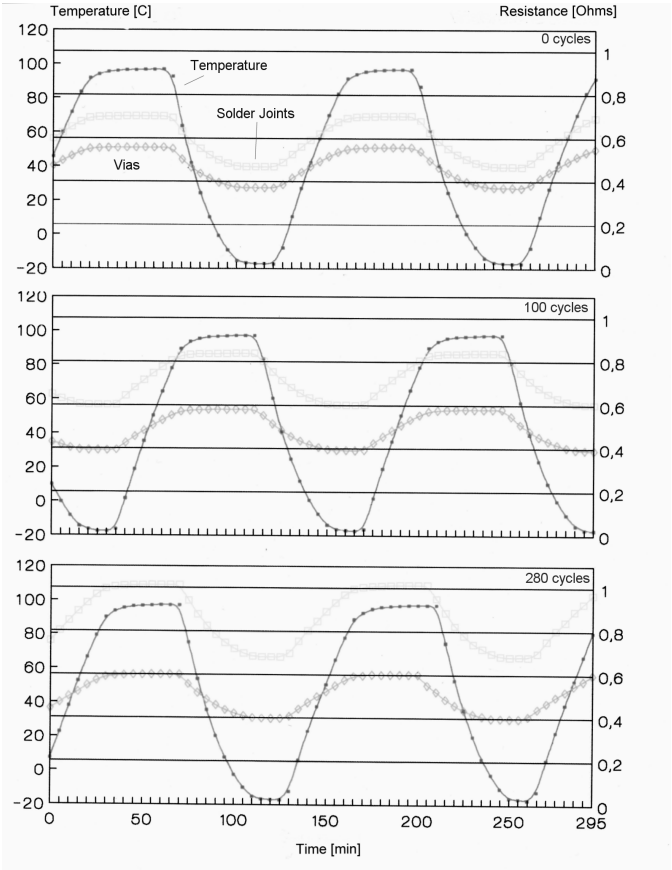

Fig. 4

Vias and solder joints were tested electrically online during temperature cycling (fig.4). For this purpose a pattern was designed, connecting 12-14 vias or solder joints in series. It can be seen in fig. 4 that the resistance of both, vias and solder joints, follows the temperature curve. However, when the behaviour after 0, 100 and 280 temperature cycles is compared, the resistance of solder joints shows an increase, whereas the resistance of the vias almost keeps stable. Though the resistance increase of the solder joints after thermal cycling is far from an elictrical failure, it indicates the creation of cracks due to thermal mismatch between the ceramic substrate and the metals involved i.e. Cu and Sn/Pb.

Packaging Options

In RML technology, layer numbers exceeding 10 can easily be established. As a demonstrator we built a 20 layers stack from .63 mm double-sided substrates with an overall height of approx. 8mm.

RML is not restricted to the metallisation methods described or to alumina ceramics only but allows the combination of various technologies and materials depending on functional demands. So, if required, ceramic layers with a higher thermal conductivity like AlN can be combined with alumina in any arrangement. Also conventional thick- or thin-

film hybrids can be mixed in the RML stack with or without electroless/electroplated substrate layers.

The RML technology offers many packaging and application options. If the bottom layer is structured as a BGA, RML modules can be mounted on PCBs directly just like other BGA components. But the RMLs can also be packed in standard plastic housings like QFP or PLCC.

An interesting housing option is the use of fully metallised outer layers of the RML stack, providing a hermetically sealed package with respect to electromagnetic radiation. Even liquid-cooled RMLs are possible with meander-like solder structures between the layers.

Conclusions

Our investigations demonstrated the feasibility of the RML technology. Its advantages vs. established LTCC technology are:

-fully processed and tested inner layers before stacking

-high potential for automation

-high flexibility with respect to design and combination of different materials

-low costs, low quality risks due to standard PCB processes

The biggest problem of RML, if metallised by electroless/electroplating, turned out to be the poor adhesion of the metallisation. So one subject for further investigations will be the improvement of the peel off strength, e.g. by a pretreatment resulting in a thin adhesion layer as the first step before metallisation.

Acknowledgments

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